# CN3882/CN3883/CN3884/CN3885
# PCB Considerations

Key words: synchronous rectification, solar charging battery, charging management

## CN3882/CN3883/CN3884/CN3885 Features

CN3882/CN3883/CN3884/CN3885 are synchronous rectifiers, compatible with solar charging management chips, with an input power supply voltage of up to 30V and a maximum charging current of 6A. Its typical application circuit is shown in Figure 1。

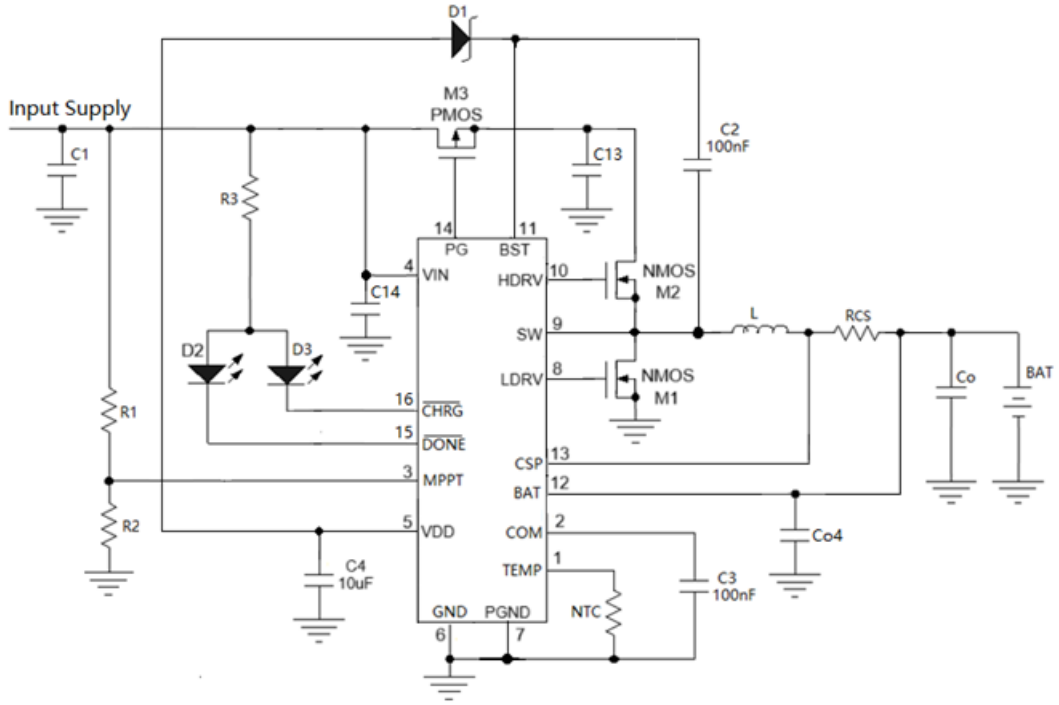


Figure 1 CN3882/CN3883/CN3884/CN3885 application circuit diagram

## Power device loop and low power device loop

In high-power loop circuits, especially those with external power devices, there are power device circuits and low-power loop circuits. In the CN3882/CN3883/CN3884/CN3885 application circuit, they are:

Power device connection terminal: C1, M3, M2, M1, l, RCS, Co, Pin7 of CN3882/CN3883/CN3884/CN3885.

Low power device connection terminal: other device ports except the above devices.

## Considerations for power device loop and low power device loop

For power device loop circuits and low-power device loop circuits, the following principles should be followed in application:

1. the power device circuit and low-power device circuit shall be separated as far as possible, and the middle shall be separated by ground wire. Try not to surround the low-power device loop area with

the power device loop area. As shown in Figure 2.

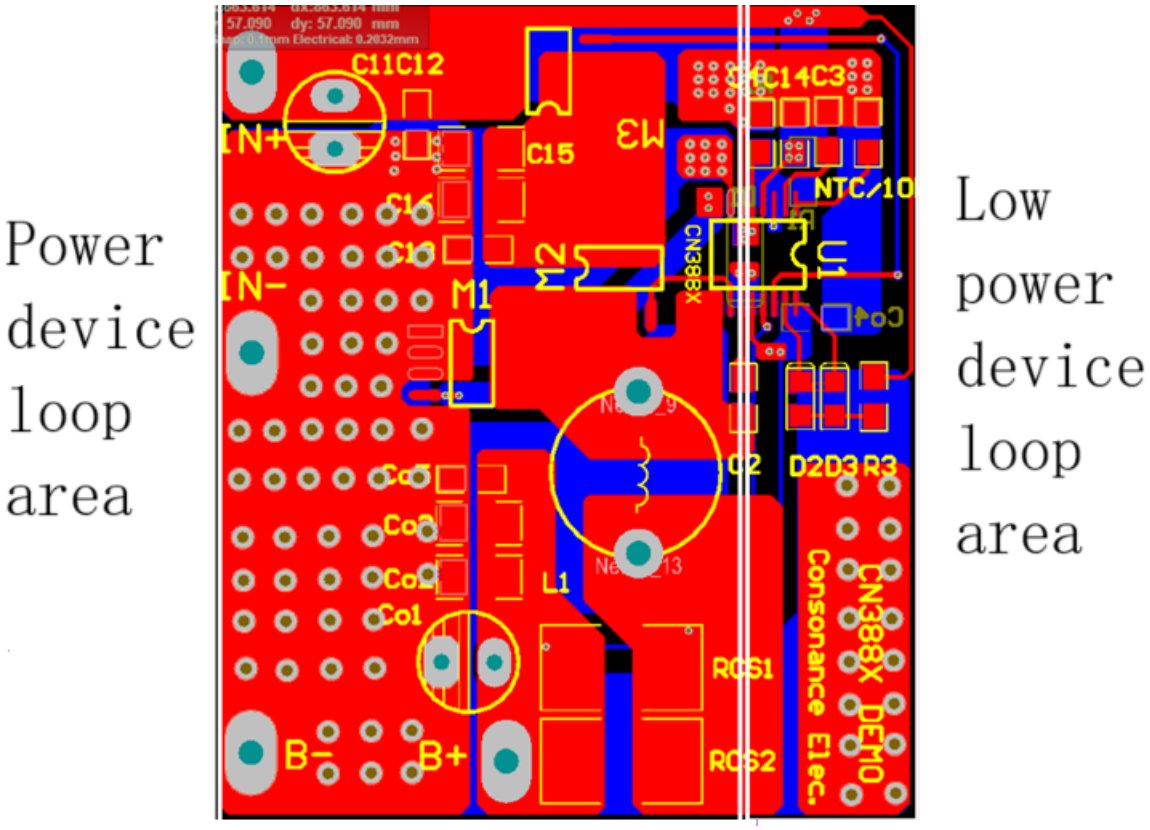


Fig. 2 Schematic diagram of separation of power device loop area and low power device loop area

2. The power device grounding terminal and the low-power device grounding terminal shall be wired to the system input capacitor grounding terminal separately. As shown in Figure 3.

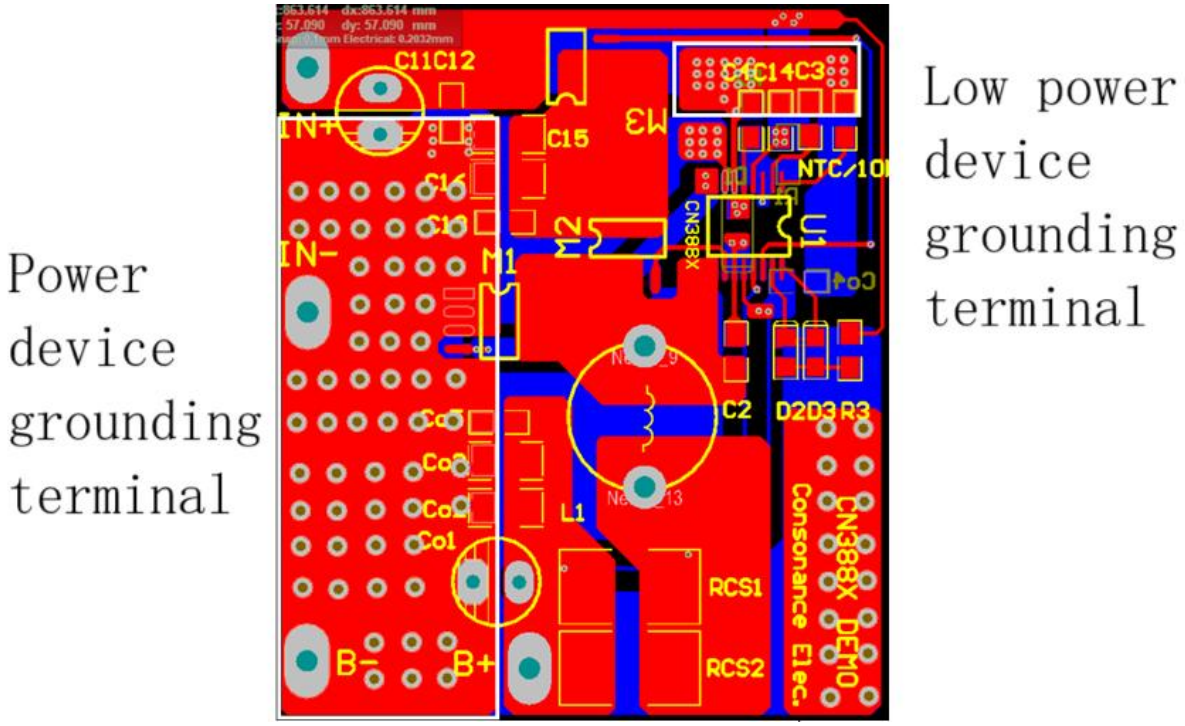


Figure 3 separate routing of power device ground wire and low power device ground wire

3. The chip input power pin VIN pin, the output battery connection pin bat pin, and a bypass capacitor C14 and Co4 should be added separately near the chip. As shown in Figure 4.

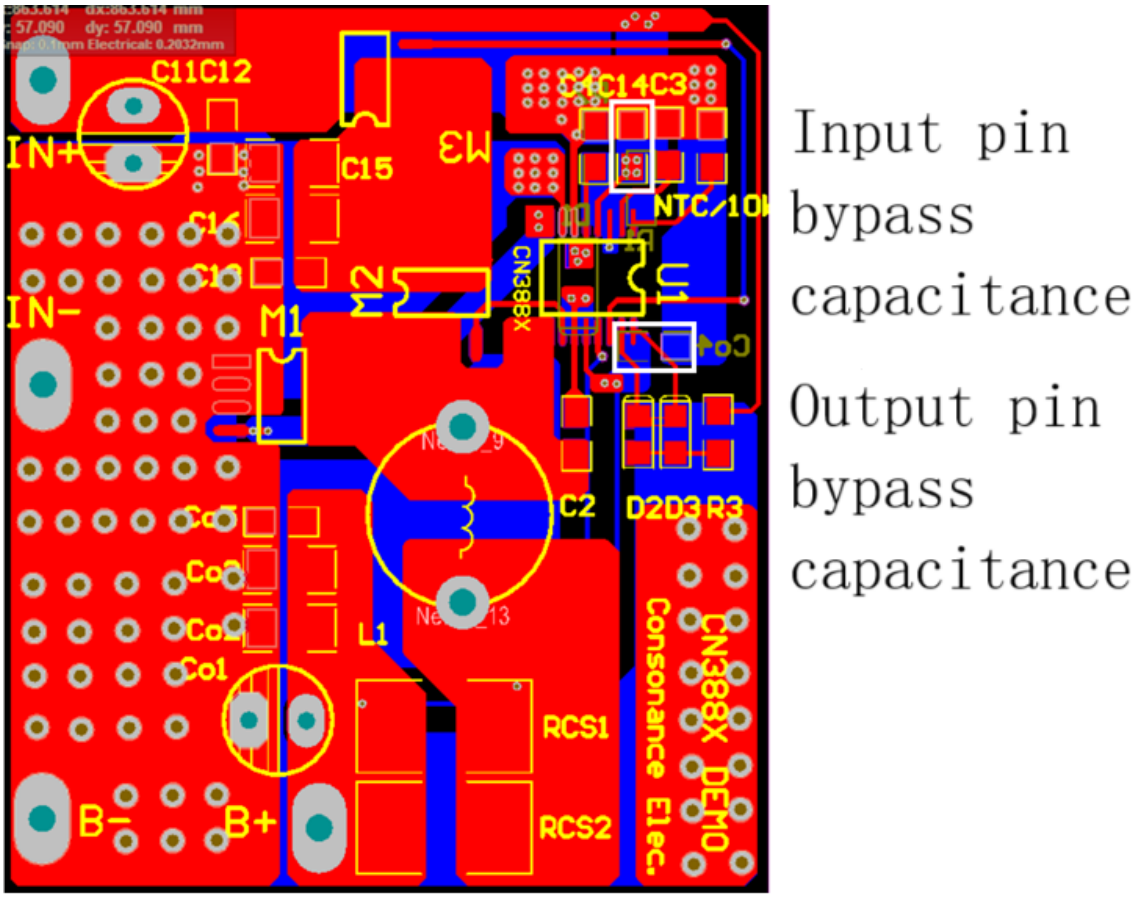


Figure 4 capacitance of VIN pin C14 and bat pin Co4 of the chip

4. The M2 gate and M1 gate should be as close to the HDRV and LDRV pins of the chip as possible, especially the M2 gate. As shown in Figure 5.

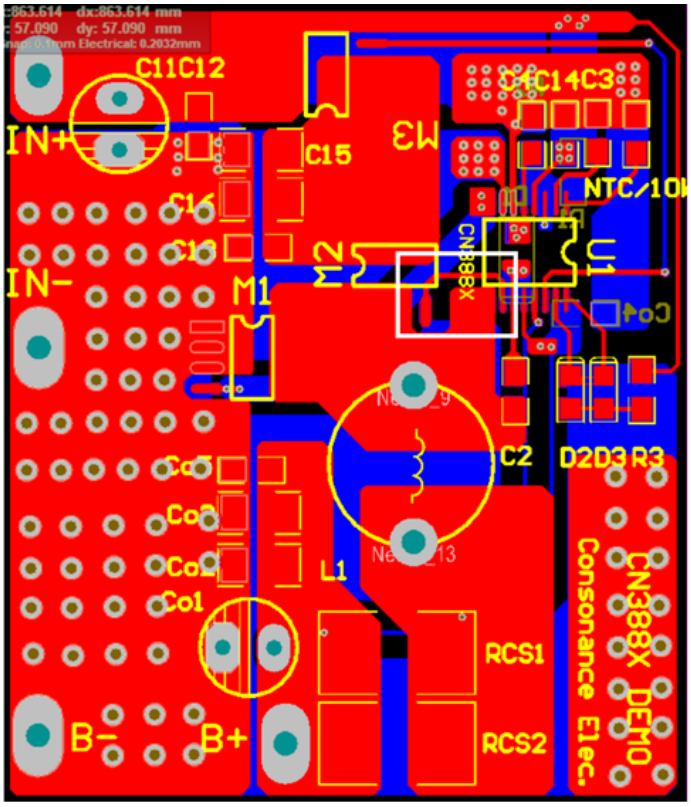


Fig. 5 the gate of M1 and M2 should be as close to the chip pin as possible

5. The two voltage dividing resistors R1 and R2 of the MPPT pin should be as close to the chip MPPT pin as possible, and the high voltage terminal of R1 should be close to the high voltage end of C14 capacitor.

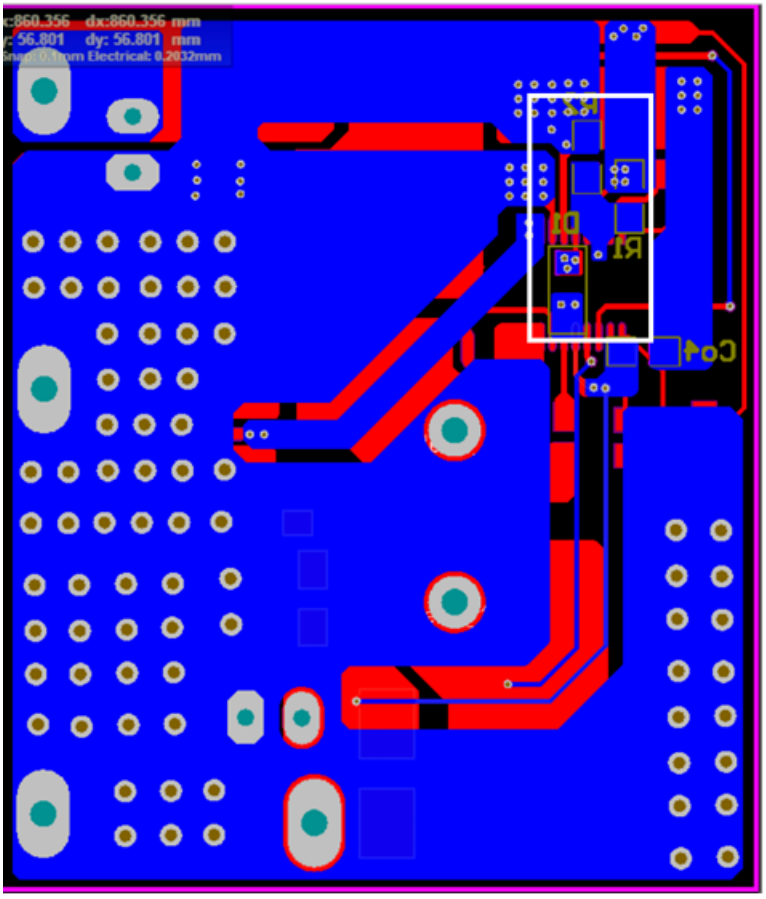


Fig. 6 the two voltage dividing resistors of MPPT pin should be as close to the pin as possible, and the R1 high voltage end should be as close to the input pin bypass capacitor as possible

6. The anode of D1 should be as close to the C4 capacitor as possible. If necessary, a capacitor can be added to the anode of D1 to the ground.

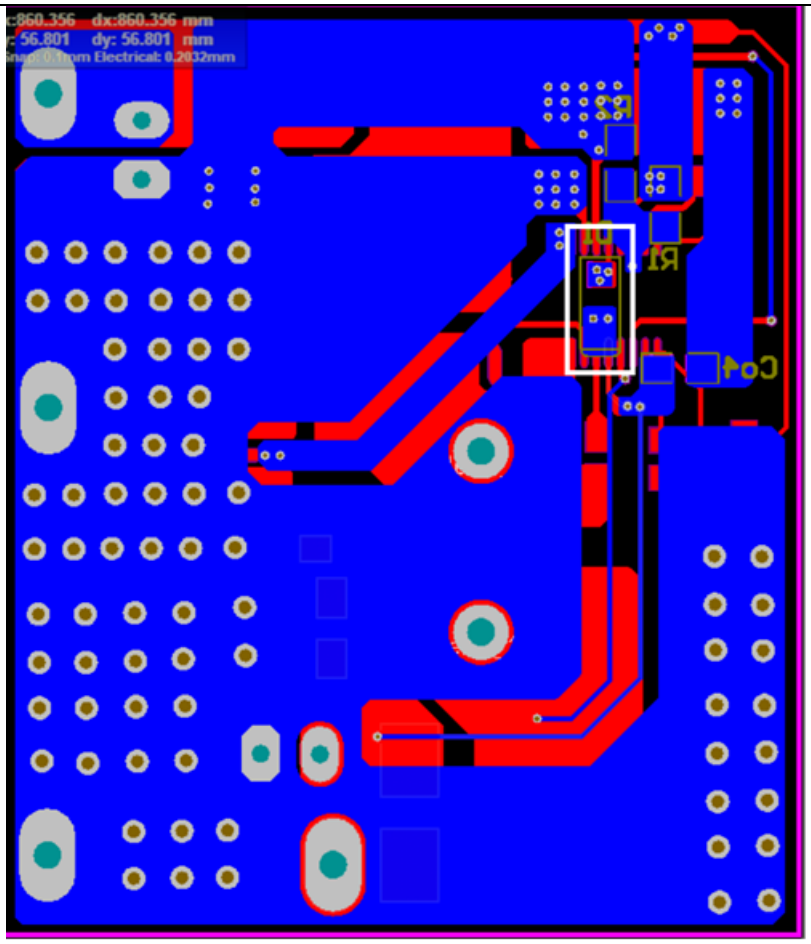


Figure 7 the anode of D1 should be as close as possible to the anode of C4